AP/2800

#10/Suppl Amend Brief 5/16/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Wilk *et al.*	Docket:	TI-24742
Serial No.:	09/176,422	Examiner:	N. Berezny
Filed:	10/21/98	Art Unit:	2823
For:	Low Temperature Method for Forming a Thin, Uniform Oxide		

SUPPLEMENTAL APPEAL BRIEF TRANSMITTAL FORM

May 10, 2002

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on May 10, 2002.

David Denker Reg. No. 40,987

Assistant Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith in triplicate is a Second Supplemental Appeal Brief in the above-identified application. This Second Supplemental Appeal Brief replaces the Supplemental Appeal Brief mailed September 5, 2001.

Applicants believe that no fee is due. However, please charge any required fee to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **Three copies of this sheet are enclosed.**

Respectfully submitted,

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SECOND SUPPLEMENTAL APPEAL BRIEF

Applicants' SECOND SUPPLEMENTAL APPEAL BRIEF is submitted to correct the deficiencies alleged in the April 23, 2002 Office Action. It is intended as a complete replacement of the SUPPLEMENTAL APPEAL BRIEF mailed September 5, 2001.

Applicants' SECOND SUPPLEMENTAL APPEAL BRIEF is submitted pursuant to 37 C.F.R. § 1.192(d) and 37 C.F.R. §1.193. Applicants mailed a REQUEST TO REINSTATE APPEAL UNDER 37 C.F.R. § 1.193 on September 5, 2001.

Applicants appeal the Examiner's rejection dated June 5, 2001, rejecting claims 1-25.

Real Party In Interest:

This application is assigned to Texas Instruments Incorporated.

Related Appeals And Interferences:

There are no related appeals or interferences.

Status of the Claims on Appeal

Claims 1-25 are pending and rejected.

Status of Amendments Filed After Final Rejection

Applicants filed a response after the final rejection. That response did not change any claims. Examiner considered the response.

Summary of the Invention

This invention pertains generally to forming thin oxides at low temperatures, and more particularly to forming thin oxides with high thickness uniformly. [1:22][1]

Process control of the growth of a 2 nm film requires unprecedented thickness control. At these thicknesses direct tunneling through the SiO2 may occur, although the effect of tunneling current on device performance may not preclude operation. Since the tunnel current depends exponentially on the dielectric thickness, small variations in process control may result in large variations in the tunnel current, possibly leading to reliability problems. [2:24 - 2:31].

Another area of concern is the interface between the gate oxide and the channel region of the substrate. This silicon dioxide/silicon interface should be very flat and uniform to help limit interface scattering of electrons in the channel region.

Rapid thermal oxidation and furnace annealing are two current methods for forming gate oxides. However, current methods do not reliably produce gate oxides with the thickness uniformity and interface smoothness that will be needed to make devices with approximately 1.5 nm, 2 nm, or 2.5 nm gate oxides practical.

We disclose a low temperature method for forming a thin gate oxide on a silicon surface. This method comprises providing a partially completed integrated circuit on a semiconductor substrate with a clean silicon surface; and stabilizing the substrate at a first temperature. The method further includes exposing the silicon surface to an atmosphere containing ozone, while maintaining the substrate at the first temperature. In this method, the exposing step creates a first, uniformly thick, gate oxide film.

Preferably, exposing the silicon surface to an atmosphere containing ozone includes exposing the silicon surface to an atmosphere containing molecular oxygen, while irradiating at

[1] [1:22] denotes page 1, line 22.

least a portion of the atmosphere with ultraviolet light, where the light transforms some of the oxygen to ozone. In some embodiments, the atmosphere further includes an inert gas, such as argon. Preferably, the ozone at the silicon surface is not in an excited energy state, such as a plasma. However, a plasma kept away from the wafer may be more acceptable. [3:1 - 3:28].

In some embodiments, the clean silicon surface is atomically flat. Typically, the semiconductor substrate contains some areas that already have some structure, such as a field oxide. In some embodiments, the substrate has a plurality of clean, atomically flat, silicon surfaces. This might occur when the gate oxide is applied to surfaces exposed by etching "windows" in a layer overlying a silicon surface; or when overlying layers are added to the silicon surface, except where "islands" have been masked off. [4:1 - 4:9].

Issues Presented for Review

The June 5, 2001 Office Action placed the new rejections before the original rejections that were at issue in the APPEAL BRIEF. This SECOND SUPPLEMENTAL APPEAL BRIEF will generally follow that sequence.

New Issues

1. Whether claims 1 - 25 contain subject matter not enabled by the specification, as required by 35 U.S.C. § 112, first paragraph.

2. Whether claims 1 - 17 and 23 contain subject matter not enabled by the specification, as required by 35 U.S.C. § 112, first paragraph.

3. Whether claims 23 - 25 contain subject matter not enabled by the specification, as required by 35 U.S.C. § 112, first paragraph.

4. Whether claim 6 contains subject matter not enabled by the specification, as required by 35 U.S.C. § 112, first paragraph.

Original Issues

5. Whether claim 18 is rendered obvious under 35 U.S.C. § 103 by the Fujishiro *et al.* patent (Fujishiro '571) in combination with the Nayar *et al.* article in ELECTRONIC LETTERS (Nayar article).

6. Whether claims 24 and 25 are rendered obvious under 35 U.S.C. § 103 by Fujishiro '571 and the Nayar article, further in view of the Wolf text, Vol. 3, p. 422-423 (Wolf text).

7. Whether claims 1 - 13—including separately patentable claim 6—are rendered obvious under 35 U.S.C. § 103 by Fujishiro '571 and the Nayar article, in view of the Choquette *et al.* patent (Choquette '687).

8. Whether claim 23 is rendered obvious under 35 U.S.C. § 103 by Fujishiro '571 and the Nayar article, in view of Choquette '687, and further in view of the Wolf text.

Grouping of Claims

Claims 1 - 5 and 7 - 17 stand and fall together. Claims 18 - 22 stand and fall together. Claims 24 - 25 stand and fall together. Claims 6 and 23 each stand independently.

ARGUMENTS REGARDING THE NEW REJECTIONS

Claims 1 - 25 are enabled by the specification

The specification teaches how to form a uniformly thick, gate oxide film

A. The Office Action asserts that the disclosure fails to enable ordinary artisans to produce uniform gate oxides. Applicants respectfully disagree.

The written description—especially pages 7 - 12 and the figures—provide detailed guidance to ordinary artisans about how to produce uniformly thick, gate oxide films. Among items specifically detailed include:

- other structures[2],
- surface preparation[3],
- temperature stabilization[4],

[2] e.g., Appl., [7:8].
[3] e.g., Appl., [7:11 - 7:25].
[4] e.g., Appl., [8:1 - 8:21].

- temperatures[5],
- pressures[6],
- oxygen concentration[7]
- electrical properties produced[8],
- ozone exposure and ozone generation[9],
- uniformity achieved and how to improve the uniformity[10],
- time dependence[11],
- etc.

Applicants submit that it is clear that these detailed descriptions of how-to-apply Applicants' method enable ordinary artisans to make uniformly thick, gate oxide films without undue experimentation. Applicants note that the scope of the claims closely corresponds to the uniformity described on page 10[12]. Additionally, the Office Action does not dispute the objective truth of the uniformities described in the specification. As such, the enabling requirement has been met.[13] Applicants request allowance of claims 1 - 25.

The Office Action does not show that Applicants' disclosed process is identical to the Nayar article's process

B. The Office Action's argument is based on the premise that Applicants' disclosed process is identical to the Nayar article's process. However, the Office Action does not show that the processes are identical. Applicants have agreed with Examiner that the processes are similar. However, Applicants respectfully disagree that the processes—as disclosed—are identical.

As noted above, Applicants give specific guidance on many aspects of their low temperature method of forming a thin gate oxide on a silicon surface. These aspects include

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[5] e.g., Appl., [8:5 - 8:9].
[6] e.g., Appl., [8:11].
[7] e.g., Appl., [8:10].
[8] e.g., Appl., [8:25].
[9] e.g., Appl., [9:1 - 9:19] and the preliminary amendment dated 9/28/98 referenced in the declaration.
[10] e.g., Appl., [10:1 - 10:14].
[11] e.g., Appl., [10:17 - 10:23].
[12] Thus this is not a case where Examiner asserts that the "scope of protection provided by that claim is not adequately enabled".
[13] A "specification disclosure which contains a teaching of the manner and process of making and using the invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as in compliance with the enabling requirement of the first paragraph of §112 unless there is reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support." Fiers v. Revel, 984 F.2d 1164, 1171; 25 U.S.P.Q.2d 1601 (Fed. Cir. 1993).

other structures, surface preparation, temperature stabilization, temperatures, pressures, oxygen concentration, electrical properties produced, ozone exposure and ozone generation, uniformity achieved and how to improve the uniformity, time dependence, etc.

The Nayar article also gives specific guidance—in at least most of these areas. If there is an area where there is no specific guidance from the Nayar article, there is no showing that the process is identical. Additionally, in some areas where both teachings give specific guidance, Applicants and the Nayar article do not always teach the same methods[14]. Given the divergence of teachings, and the unknown amount of overlap in some areas—it is not surprising that the results achieved differ.

The Appeal Brief does not state that Nayar's process cannot produce uniformly thick gate oxides.

C. Applicants agent has not admitted that "ordinary artisans would not succeed in using Nayar to produce a uniformly thick gate oxide." Instead, the Appeal Brief states

- "The Nayar article does not mention that the oxide is highly uniform. Instead, the article mentions that the thickness measurements are averages. Additionally, an examination of the Nayar article fig. 2 shows that at 250° C, the oxide thickness may not be well behaved. Ordinary artisans would not be assured that the Nayar article oxides had sufficient thickness uniformity for a conventional gate oxide."[15]
- "However, there is no evidence that the Nayar article's useful method creates uniformly thick layers—to which Applicants' claims are limited."[16]
- "Applicants submit that uniform thickness is not an inherent property of an ordinary oxide. Thus, there is no evidence that the cited references teach how to achieve a critical limitation of the claim."[17]
- "Additionally, there is no evidence that the postulated combination achieves a critical limitation of the claim—that the gate oxide be uniformly thick."[18]

These statements do not pass judgment upon the thickness uniformity of the Nayar article method. Instead, they are argument about what the Nayar article would teach an ordinary artisan—before the artisan duplicated Nayar's method in their own lab.

[14] e.g., surface preparation, temperature stabilization, and pressures.
[15] Brief, [4:20].
[16] Brief, [5:8].
[17] Brief, [5:13].
[18] Brief, [8:5].

Claims 1 - 17 and 23 are enabled by the specification

The specification incorporates Appl. No. 08/904,009 by reference

D. The Office Action asserts that the disclosure fails to enable ordinary artisans to produce "clean atomically flat, silicon surfaces". Applicants respectfully disagree. Page 1, line 15 of the application incorporates by reference another application by Wilk *et al*—TI-22960, filed 7/31/97, titled "Method For Thin Film Deposition On Single-Crystal Semiconductor Substrates". This referenced application has since matured into patent 6,020,247. Method For Thin Film Deposition On Single-Crystal Semiconductor Substrates fully discloses how to make clean, atomically flat, silicon surfaces. A copy of the patent is enclosed for the Board's convenience. Applicants request allowance of claims 1 - 17 and 23.

Claims 23 - 25 are enabled by the specification

Applicants teach a method of forming oxides with greater than 10 MV/cm breakdown voltage.

E. The Office Action notes that the disclosure fails to disclose which process variations would enable ordinary artisans to control the breakdown voltage.

Applicants' disclosure states "This ozone-based method can routinely achieve breakdown voltages above 10 MV/cm, such as 12 to 13 MV/cm." Ordinary artisans will understand that the breakdown voltages achieved will vary somewhat—both from lot-to-lot, and as process parameters are varied. Applicants have given detailed guidance on some process parameter variations and general guidance on others. The lack of specific guidance on how to control the breakdown voltage does not prevent the specification from enabling the claimed invention. Applicants request allowance of claims 23 - 25.

Claim 6 is enabled by the specification

Applicants teach how to form oxides using energetic ozone sources

F. The Office Action asserts that "wherein at least part of the atmosphere that does not contact the silicon surface includes an ozone plasma" is not enabled. Applicants clearly teach how to practice the invention—even if the ozone source is energetic.[19]

Applicants did not state that ordinary artisans could not use the Nayar article's method to produce the claimed limitation. Instead, Applicants stated "Applicants do not see where the cited art teaches or suggests using a remote ozone plasma. Instead, the Nayar article teaches a UV/ozone method to oxidize silicon."[20]

These statements do not pass judgment upon the whether the Nayar article could be combined with an ozone plasma. Instead, they are argument about what the Nayar article would teach an ordinary artisan. Applicants request allowance of claim 6.

ARGUMENTS REGARDING THE ORIGINAL REJECTIONS

Fujishiro '571 and the Nayar article do not render claim 18 obvious

Ordinary artisans would not have a reasonable expectation of success

G. Claim 18's limitations include—among others—"exposing the silicon surface to an atmosphere including ozone, while maintaining the substrate at the first temperature, wherein the exposing step creates a first, uniformly thick, **gate oxide** film".

The Nayar article teaches a method of growing oxide layers. However, these oxides were not used as gate oxides. The article notes that the fixed oxide charges are high[21], and that the typical breakdown field is approximately 4 MV/cm[22]. The Office Action implied that the GATE OXIDE CHARACTERISTICS NEEDED FOR SUBMICRON MOSFETS section of the Wolf text

[19] "Energetic ozone sources can be used, but it is preferable to keep the any excited ozone species from contacting the wafer." Appl. [9:7].
[20] Brief [7:13].
[21] Nayar article, [206:first full paragraph].
[22] *id.*

lists characteristics that ordinary artisans would understand are necessary for/inherent in a conventional MOSFET gate oxide. Three of these characteristics are:

2. The specified oxide thickness must also be sufficiently uniform across the entire wafer, and from wafer to wafer, and from run-to-run.

3. The gate oxide film and the Si/SiO_2 interface must exhibit adequately small values of charge in the oxide and at the $Si-SiO_2$ interface. (i.e., low Q_f, D_{it}, Q_{ot} and Q_m values - see chap. 3).

4. The dielectric breakdown strength of the oxide must be sufficiently high (e.g., >8 MV/cm), implying that the film is pinhole free and contains a negligible number of defects that would lead to oxide breakdown at lower electric fields.[23]

The Nayar article explicitly teaches that its oxides have high fixed charges. Thus, ordinary artisans would understand that the Nayar article oxides would not be suitable for a conventional gate oxide. The Nayar article explicitly teaches that its oxides breakdown near 4 MV/cm. Thus, ordinary artisans would understand that the Nayar article oxides would not be suitable for a conventional gate oxide. The Nayar article does not mention that the oxide is highly uniform. Instead, the article mentions that the thickness measurements are averages. Additionally, an examination of the Nayar article fig. 2 shows that at 250° C, the oxide thickness may not be well behaved. Ordinary artisans would not be assured that the Nayar article oxides had sufficient thickness uniformity for a conventional gate oxide.

In short, Applicants submit that an ordinary artisans would not consider an approach based on the Nayar article to have a reasonable expectation of success.[24] Without this expectation of success, obviousness has not been shown.

<u>The postulated combination does not teach how to achieve a critical limitation of the claim</u>

H. Applicants' claim 18 limitations also include the requirement that the gate oxide be uniformly thick. Nayar's useful method of forming extremely thick oxide layers at low temperatures makes no mention of obtaining uniform thicknesses. Instead, the Nayar article states

[23] Wolf text, [422].

that the thickness data is an average of several measurements[25]. Applicants submit that if Nayar had found high thickness uniformity (such as Applicants' <3% uniformity), the Nayar article would have reported the achievement. However, there is no evidence that the Nayar article's useful method creates uniformly thick layers—to which Applicants' claims are limited.

As Applicants understand it, the Office Action submits that uniformly thick layers would be an inherent property of a gate oxide. This may often be true. However, the Nayar article does not form gate oxides. Instead, it forms oxide films that are not suitable for use as gate oxides[26]. Applicants submit that uniform thickness is not an inherent property of an ordinary oxide. Thus, there is no evidence that the cited references teach how to achieve a critical limitation of the claim.

Applicants submit that the claims are patentable over the cited references because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of independent claim 18 and its dependants.

Fujishiro '571, the Nayar article, and the Wolf text do not render claims 24 and 25 obvious

I. Applicants arguments for claim 18 above are equally applicable to claims 24 and 25, and are repeated here by reference.

Applicants note that the Office Action alleges that these claims do not further limit the scope of claim 18. Applicants disagree with this objection. Claim 24 is exemplary. Claim 24 further limits claim 18, in that it limits the types of methods of forming thin gate oxides on silicon surfaces that would infringe this claim. Applicants submit that a process—that used the other steps in the claim—to make a gate oxide with a breakdown strength of 8 MV/cm would infringe claim 18, but not infringe claim 24.

The postulated combination does not teach how to achieve a critical limitation of the claims

J. Claims 24 and 25 are further limited to methods that create gate oxide films with breakdown voltages greater than 10 MV/cm or 12 MV/cm. The Nayar article that was cited as a similar process does not teach a method capable of forming gate oxide films with these

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[24] "Obviousness does not require absolute predictability, but a reasonable expectation of success is necessary." -- In Re Clinton, 188 U.S.P.Q. 365 (CCPA, 1976).
[25] Nayar article [206:3].
[26] See argument G, *supra*.

breakdown voltages. The other cited references do not seem to cure this deficiency either.

Applicants submit that the claims are patentable over the cited references because of their dependence from a valid base claim, and because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of claims 24 and 25.

Fujishiro '571, the Nayar article, and Choquette '687 do not render claims 1 - 13 obvious

K. Applicants arguments for claim 18 above are equally applicable to claim 1, and are repeated here by reference.

Ordinary artisans would not reasonably expect Choquette '687's GaAs process to produce the claimed atomically flat, silicon surface

L. Claim 1's limitations also include "providing a partially completed integrated circuit on a semiconductor substrate with a clean, **atomically flat, silicon surface**". Choquette '687 teaches a useful process for removing surface contaminants such as C, Si and O, from substrates of the gallium arsenide or indium phosphide families. Applicants have studied Choquette '687—including the abstract section cited—and have not found where it teaches a method of forming an atomically flat Si surface. The abstract does mention that this method forms an atomically smooth semiconductor surface. However, when read in context with the rest of the disclosure, Applicants submit that Choquette '687 enables forming atomically smooth surfaces on III-IV semiconductors, such as gallium arsenide, indium phosphide, and the like. Applicants submit that ordinary artisans would not reasonably expect a method to remove Si from a GaAs surface would be useful to form the claimed atomically flat, silicon surface. As such, obviousness has not been established.

Applicants also disagree with Examiner's assertion that ordinary artisans would be clearly motivated to provide an atomically flat surface. The cited references do not indicate that this type of surface is required. In the absence of a need for an atomically flat surface, ordinary artisans would be motivated to eliminate unnecessary steps in order to reduce costs.

Applicants submit that the claims are patentable over the cited references because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of independent claim 1 and its dependents.

Claim 6 has additional limitations

M. Claim 6 is dependant upon claim 1, and is allowable since the base claim is allowable. However claim 6 has additional limitations not taught or suggested by the cited art. These limitations include "exposing the silicon surface to an atmosphere with less energy than a plasma", and wherein "at least part of the atmosphere that does not contact the silicon surface includes an ozone plasma."

Applicants do not see where the cited art teaches or suggests using a remote ozone plasma. Instead, the Nayar article teaches a UV/ozone method to oxidize silicon.

Applicants submit that claim 6 is are patentable over the cited references because of it dependence from a valid base claim, and because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of claim 6.

Fujishiro '571, the Nayar article, Choquette '687, and the Wolf text do not render claim 23 obvious

N. Applicants arguments for claims 18, 24, and 1 above are equally applicable to claim 23 and are repeated here—in combination—by reference.

Applicants submit that claim 23 is are patentable over the cited references because of it dependence from a valid base claim, and because the references do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of claim 23.

CONCLUSION

Claims 1 - 25 are enabled by the specification. The written description provides detailed guidance to ordinary artisans about how to produce uniformly thick, gate oxide films. The scope of the claims closely corresponds to the uniformity described on page 10. The Office Action does not dispute the objective truth of the uniformities described in the specification. Additionally, the Office Action does not show that Applicants' disclosed process is identical to the Nayar article's process.

Claims 1 - 17 and 23 are enabled by the specification. The specification incorporates Appl. No. 08/904,009 by reference.

Claims 23 - 25 are enabled by the specification. Applicants teach a method of forming oxides with greater than 10 MV/cm breakdown voltage.

Claim 6 is enabled by the specification. Applicants teach how to form oxides using energetic ozone sources.

Original Rejections

Claim 18 and its dependants are patentable over Fujishiro '571 and the Nayar article. Ordinary artisans would not have a reasonable expectation of success since the Nayar article teaches oxides that do not have characteristics that ordinary artisans look for in a conventional gate dielectric. Additionally, there is no evidence that the postulated combination achieves a critical limitation of the claim—that the gate oxide be uniformly thick.

Claims 24 and 25 are patentable over Fujishiro '571, the Nayar article, and the Wolf text. The postulated combination does not teach how to achieve another critical limitation of the claims—that the method create gate oxide films with breakdown voltages greater than 10 MV/cm or 12 MV/cm.

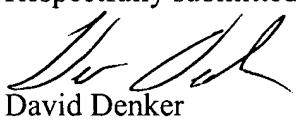
Claim 1 and its dependants are patentable over Fujishiro '571, the Nayar article, and Choquette '687. The arguments for claim 18 above are equally applicable to claim 1, and ordinary artisans would not reasonably expect Choquette '687's GaAs process to produce the claimed atomically flat, silicon surface. Claim 6 is dependant upon an allowable base claim, and the cited art does not teach or suggest a remote ozone plasma.

Claim 23 is patentable over Fujishiro '571, the Nayar article, Choquette '687, and the Wolf text. The arguments in favor of claims 18, 24, and 1—in combination—show that claim 23 is patentable.

Applicants believe that the application is in condition for allowance. However, should the honorable Board have any comments or suggestions, Applicant respectfully requests that the honorable Board contact the undersigned in order to quickly resolve any outstanding issues.

Please charge any required fee to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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FORM PTO-1449 (REV. 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*	TI-24742	09/176,422
	APPLICANT Wilk *et al.*	
	FILING DATE 10/21/98	GROUP 2823

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	AA						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	BA							

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

NB	CA	Nayar, et al., "Chemically Treated Stepped Silicon {100} Surfaces," Proceedings of the International Symposium on the Ultra-Clean Processing of Silicon Surfaces, 19 September 1994, pp. 371-374 (VISHAL NAYAR, ALLAN J . PIDDUCK, MOHAMMED IDREES and BEVERLEY E.J. DEW)
NB	CB	V. Nayar, et al., "Atmospheric Pressure, Low Temperature (<500°C) UV/Ozone Oxidation of Silicon," Electronic Letters, 1 February 1990, Vol. 26, No. 3, pp. 205-206 (V. NAYAR, P. PATEL, IAN W. BOYD)
NB	CC	Morita, et al., "Effects of Si Wafer Surface Micro-Roughness on Electrical Properties of Very-Thin Gate Oxide Films," Proceedings of the International Symposium on Ultra Large Scale Integration Science and Technology, Pennington, NJ, 5 May 1991, pp. 400-408 (M. MORITA, A. TERAMOTO, K. MAKIHARA, and T. OHMI)
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NB	CE	Chin, et al., "Thin Oxides With In-Situ Native Oxide Removal," IEEE Electron Device Letters, IEEE Inc. New York, Vol. 18, No. 9, 1 September 1997, pp. 417-419 (ALBERT CHIN, SENIOR MEMBER IEEE, W. J. CHEN, T. CHANG, R.H. KAO, B.C. LIN, TSAI and J.C.-M HUANG)
NB	CF	Froeschle, et al., "Cleaning Process Optimization in a Gate Oxide Cluster Tool Using an In-Line XPS Module," Mat. Res. Soc. Symp., Proc. Vol. 477, 1 April 1997, pp. 371-377 (BARBARA FROESCHLE, FREDERIQUE GLOWACKI, ANTON J. BAUER, IGOR KASKO, RICHARD OECHSNER and CLAUS SCHNEIDER)
NB	CG	Nakanishi, et al., "Ultrathin Oxides by UV/Ozone Pretreatment Cleaning and Ozone Oxidation," Proceedings of the International Symposium of the Physics and Chemistry of SOi_2 and the Si-SiO_2 Interface, Vol. 96, No. 1, 5 May 1996, pp. 316-328 (TOSHIRO NAKANISHI, SATOSHI OHKUBO, YASUYUKI TAMURA, RINJI SUGINO, NAOKI AWAJI, and KANETAKE TAKASAKI)
NB	CH	Nayar, et al., "An Effective Oxidation Technique for the Formation of Thin SiO_2 at <500°C," Insulating Films on Semiconductors 1991 Proceedings from the 7th Biennial European Conference Including Satellite Workshops on Silicon on Insulator: Materials and Device Technology and the Physics of Hot Electron Degradation in Si Mosfets Liverpoo, pp. 163-166 (VISHAL NAYAR and IAN W. BOYD)
NB	CI	Nakanishi, et al., "Oxidation in Ozone," Fujitsu-Scientific and Technical Journal, Fujitsu Limited, Kawasaki, JP, Vol. 32, No. 1, 1 June 1996, pp. 128-131 (TOSHIRO NAKANISHI, SATOSHI OHKUBO and YASUYUKI TAMURA)

EXAMINER	DATE CONSIDERED
Neal Berezny	7/26/02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.